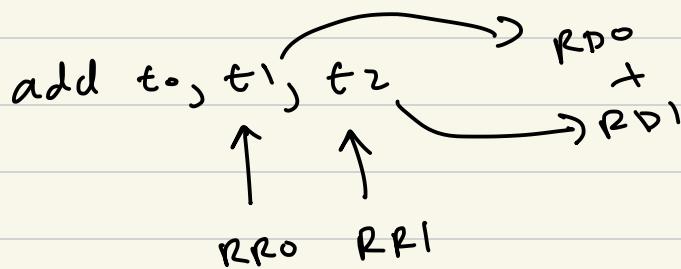
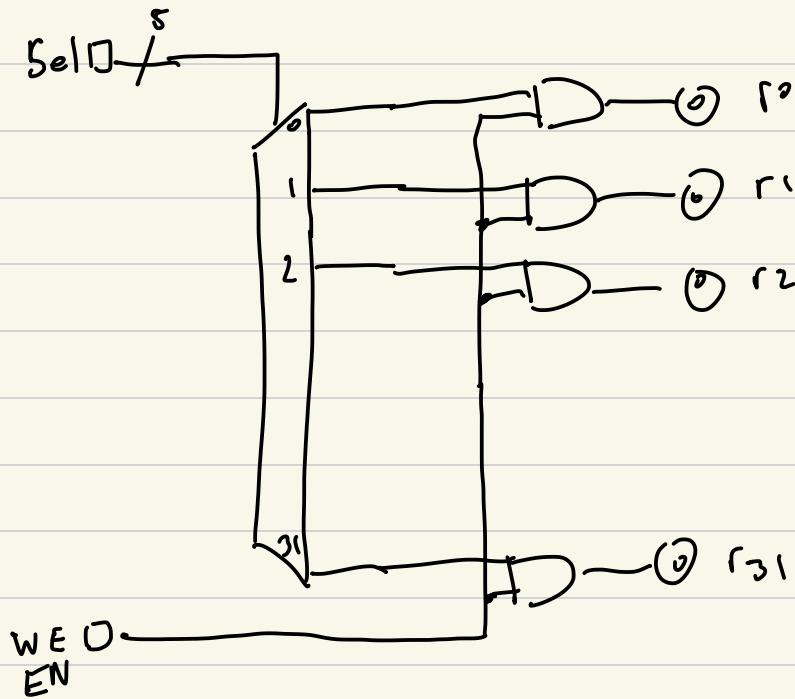


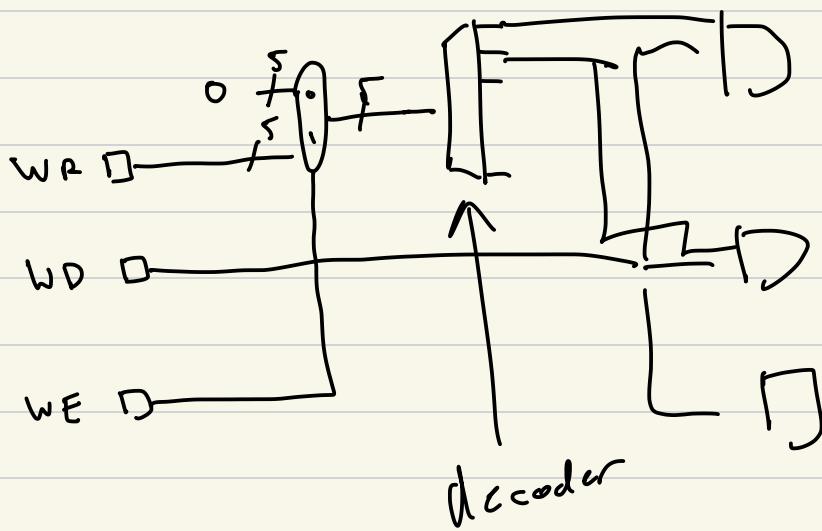
# C5315-01 Lab Processor Design ALU



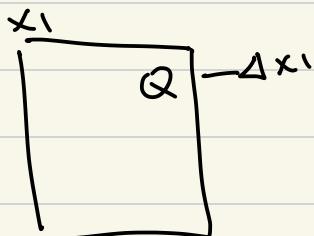
Decoder with Enable



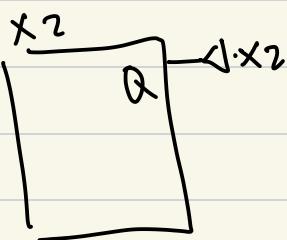
# Alternative Approach



$x_0 \quad 0 \longrightarrow \Delta x_0$



$x_0 \triangleright -$   
 $x_1 \triangleright -$   
 $x_2 \triangleright -$   
— ⊙ RD<sup>0</sup>

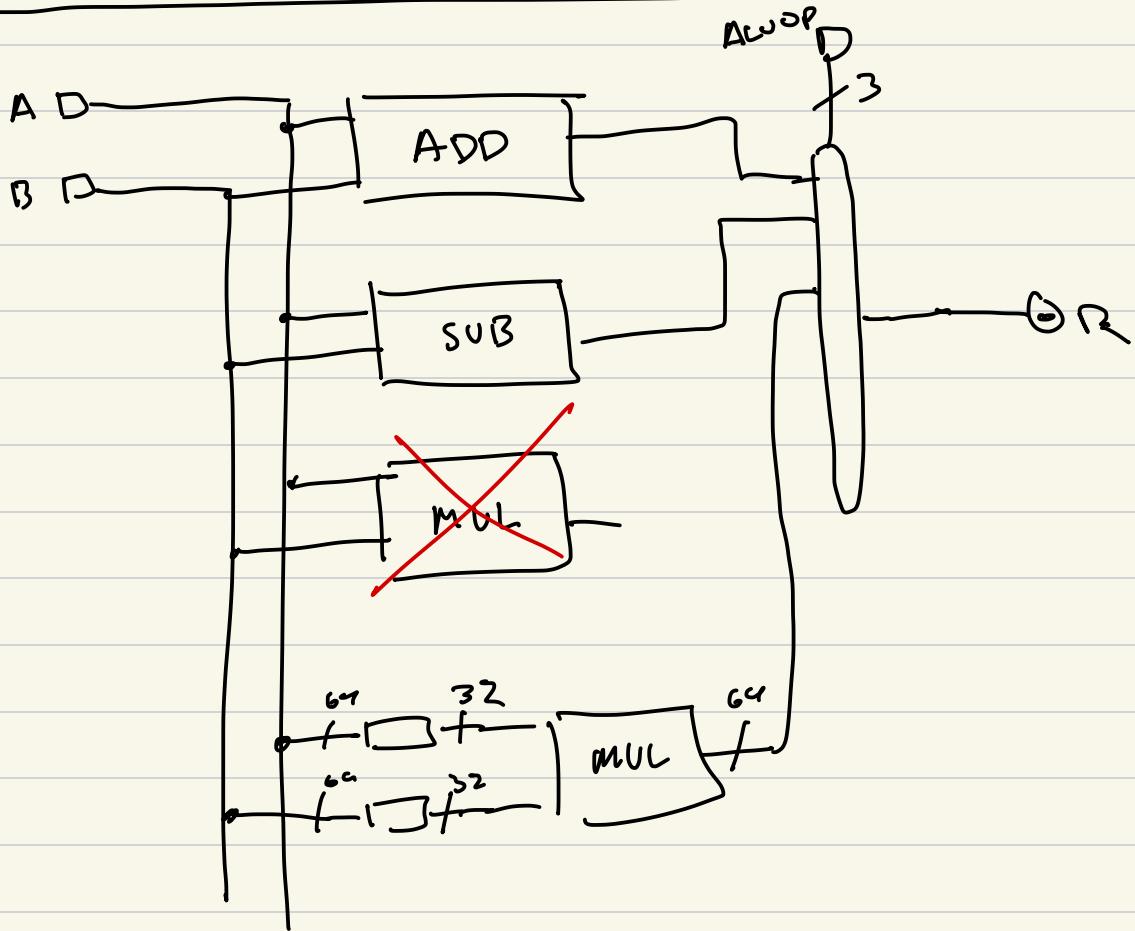
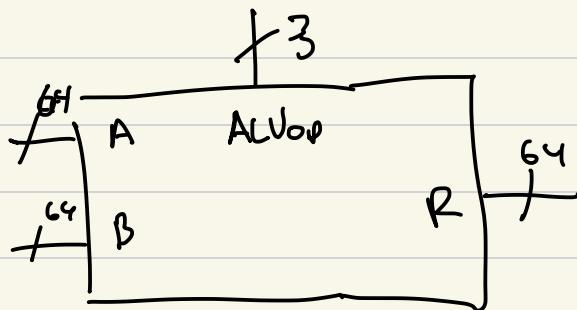


$x_0 \triangleright -$   
 $x_1 \triangleright -$   
 $x_2 \triangleright -$   
 $x_3 \triangleright -$   
— ⊙ RD<sup>1</sup>

$x_0 \triangleright -$   
 $x_1 \triangleright -$   
 $x_2 \triangleright -$   
— ⊙ RD<sup>1</sup>

$x_3 \triangleright -$

# ALU Arithmetic Logic Unit



li t<sub>0</sub>, 3

li t<sub>1</sub>, 8

add t<sub>1</sub>, t<sub>0</sub>, t<sub>1</sub>