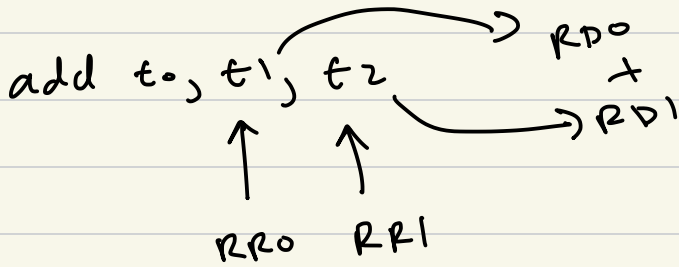
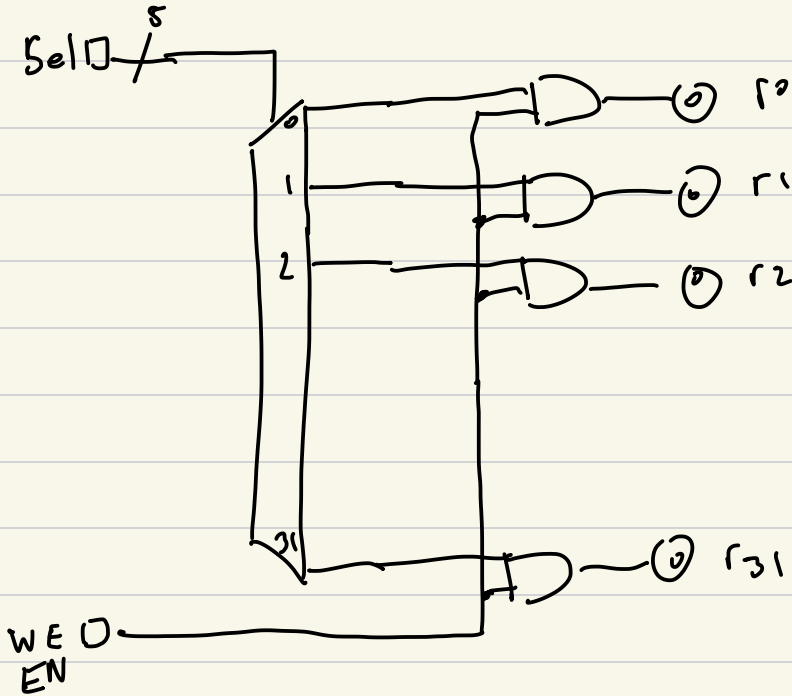


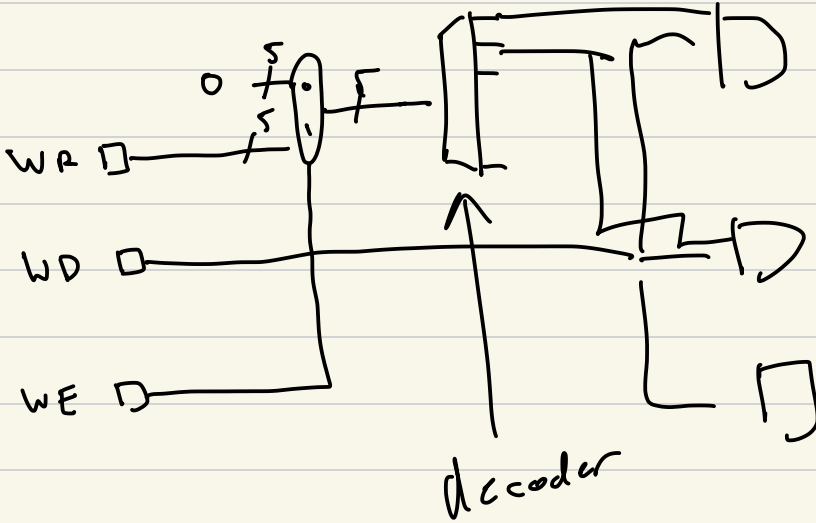
CS315-01 Lab Processor Design ALU



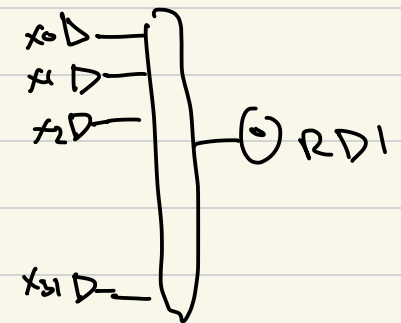
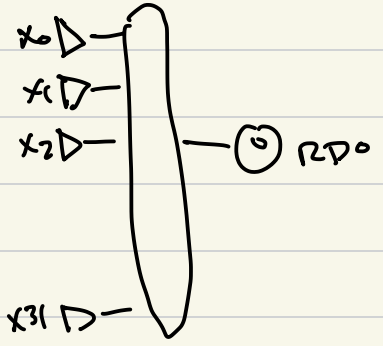
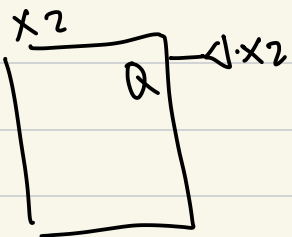
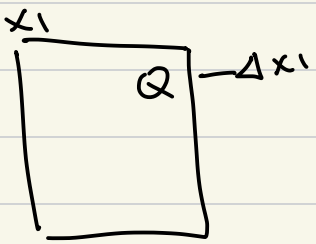
Decoder with Enable



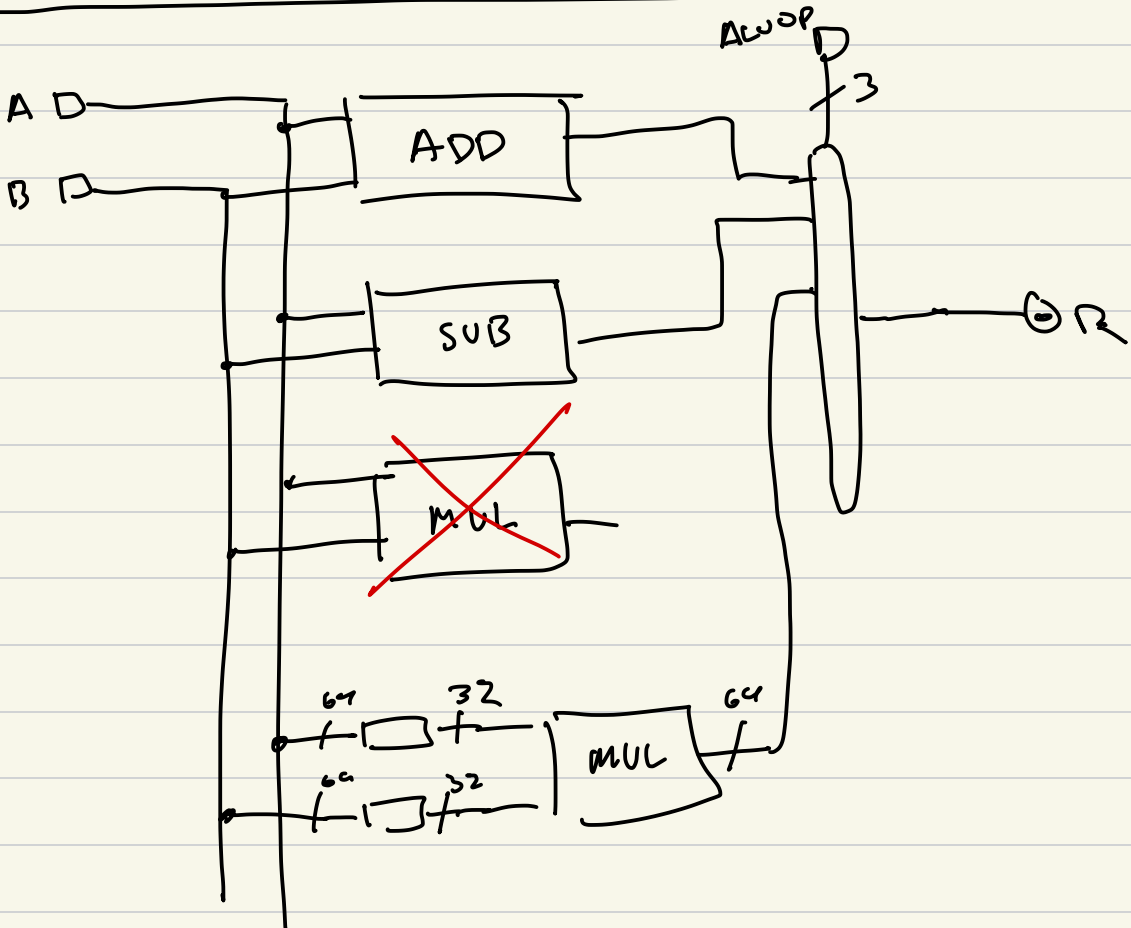
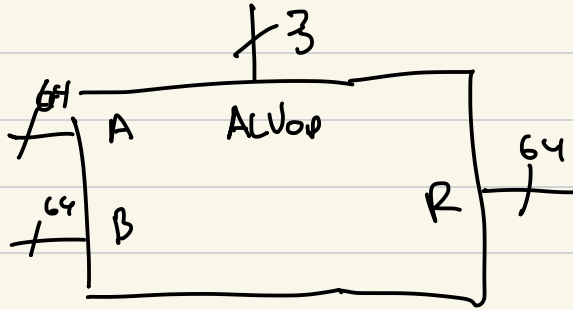
Alternative Approach



$x_0 \quad 0 \quad \Delta x_0$



ALU Arithmetic Logic Unit



li t0, 3

li t1, 8

add t1, t0, t1